

What is claimed is:

- 1 1. A plasma display device comprising:
 - 2 at least one fiber structure including a conductive electrode inside or on a surface
 - 3 of the fiber; and
 - 4 an erase address drive control system, wherein said erase address drive control
 - 5 system includes:
 - 6 means for storing a charge on each subpixel to turn each subpixel ON; and
 - 7 means for selectively removing said charge from at least one subpixel by
 - 8 applying an erase pulse to its corresponding electrodes, thereby
 - 9 turning said at least one subpixel OFF.
- 1 2. A plasma display device according to claim 1, further comprising a ramped voltage
 - 2 address drive control system wherein said ramped voltage address drive control
 - 3 system includes:
 - 4 means for turning each subpixel ON by applying at least one voltage ramp to at
 - 5 least one pair of sustain electrodes to create a standardized charge at each
 - 6 subpixel; and
 - 7 means for selectively removing said charge from at least one subpixel by applying
 - 8 an erase pulse to its corresponding electrodes, thereby turning said at least
 - 9 one subpixel OFF.
- 1 3. A plasma display device comprising:
 - 2 at least one fiber structure including a conductive electrode inside or on a surface
 - 3 of the fiber; and
 - 4 a write address drive control system wherein said write address drive control
 - 5 system includes:

6 means for removing a charge from each subpixel, thereby turning each
7 subpixel OFF; and

8 means for adding charge to at least one subpixel by applying a voltage to its
9 corresponding electrodes, thereby turning said at least one subpixel ON.

1 4. A plasma display device comprising:

2 at least one fiber structure including a pair of barrier ribs that define a plasma
3 channel, at least one wire address electrode inside or on a surface of said
4 fiber, and a phosphor layer coating on said surface of said plasma channel;

5 a glass plate with patterned sustain electrodes; and

6 an erase address drive control system, wherein said erase address drive control
7 system includes:

8 means for storing a charge over said sustain electrodes on each subpixel to
9 turn each subpixel ON; and

10 means for selectively removing said charge from at least one subpixel by
11 applying an erase pulse to its corresponding wire address electrode,
12 thereby turning said at least one subpixel OFF.

1 5. A plasma display device according to claim 4, further comprising a ramped voltage
2 address drive control system wherein said ramped voltage address drive control
3 system includes:

4 means for turning each subpixel ON by applying at least one voltage ramp to at
5 least one pair of sustain electrodes to create a standardized charge at each
6 subpixel; and

7 means for selectively removing said charge from at least one subpixel by applying
8 an erase pulse to its corresponding wire address electrode, thereby turning
9 said at least one subpixel OFF.

1 6. A plasma display device comprising:

at least one fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel;

a glass plate with patterned sustain electrodes; and

a write address drive control system wherein said write address drive control system includes:

means for removing a charge from each subpixel, thereby turning each subpixel OFF; and

means for adding charge to at least one subpixel by applying a voltage to its corresponding sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

7. A plasma display device comprising:

at least one first fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel;

at least one second fiber structure including at least one wire sustain electrode located near a surface of said first fiber; and

an erase address drive control system, wherein said erase address drive control system includes:

means for storing a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

means for selectively removing said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

8. A plasma display device according to claim 7, further comprising a ramped voltage address drive control system wherein said ramped voltage address drive control system includes:

means for turning each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and

means for selectively removing said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

9. A plasma display device comprising:

at least one fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel;

at least one second fiber structure including at least one wire sustain electrode located near a surface of said first fiber; and

a write address drive control system wherein said write address drive control system includes:

means for removing a charge from each subpixel, thereby turning each subpixel OFF; and

means for adding charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

10. A surface discharge plasma display device, comprising:

a first glass plate comprising a plurality of sustain electrodes, a thin dielectric layer covering said sustain electrodes and an emissive film covering said dielectric layer;

a fiber array including a plurality of fibers, each bottom fiber including a pair of barrier ribs that define a plasma channel, at least one wire address electrode located near a surface of said plasma channel, and a phosphor layer coating on said surface of said plasma channel; and

a second glass plate, wherein said fiber array is sandwiched between said first glass plate and said second glass plate; and

said plasma display being hermetically sealed with a glass frit around a perimeter of the first and second glass plates and said wire address electrodes are brought out through said glass frit for direct connection to a drive control system;

wherein said drive control system is selected from the group consisting of:

- a) an erase drive control system;
- b) a write address drive control system; and
- c) a ramped voltage address drive control system.

11. The surface discharge plasma display device of claim 10, wherein said erase drive control system includes:

means for storing a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

means for selectively removing said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

12. The surface discharge plasma display device of claim 10, wherein said write address drive control system includes:

means for removing a charge from each subpixel, thereby turning each subpixel OFF; and

means for adding charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

13. The surface discharge plasma display device of claim 10, wherein said ramped voltage drive control system includes:

means for turning each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and

means for selectively removing said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

14. A surface discharge plasma display device, comprising:

two glass plates sandwiched around first and second orthogonal arrays of fibers defining a structure of said display;

said first fiber array including a plurality of top fibers, each top fiber including at least one pair of wire sustain electrodes located near a surface of said top fiber, said surface being covered by an emissive film;

said second fiber array including a plurality of bottom fibers, each bottom fiber including a pair of barrier ribs that define a plasma channel, at least one wire address electrode located near a surface of said plasma channel, and a phosphor layer coating on said surface of said plasma channel; and

said plasma display being hermetically sealed around a perimeter of the glass plates with a glass frit and said pair of wire sustain electrodes and said wire address electrode are brought out through said glass frit for direct connection to a drive control system;

wherein said drive control system is selected from the group consisting of:

- 16 a) an erase drive control system;
- 17 b) a write address drive control system; and
- 18 c) a ramped voltage address drive control system..

1 15. The surface discharge plasma display device of claim 14, wherein said erase drive
2 control system includes:

3 means for storing a charge over said sustain electrodes on each subpixel to turn
4 each subpixel ON; and

5 means for selectively removing said charge from at least one subpixel by applying
6 an erase pulse to its corresponding wire address electrode, thereby turning
7 said at least one subpixel OFF.

1 16. The surface discharge plasma display device of claim 14, wherein said write address
2 drive control system includes:

3 means for removing a charge from each subpixel, thereby turning each subpixel
4 OFF; and

5 means for adding charge to at least one subpixel by applying a voltage to its
6 corresponding wire sustain electrodes and wire address electrode, thereby
7 turning said at least one subpixel ON.

1 17. The surface discharge plasma display device of claim 14, wherein said ramped voltage
2 drive control system includes:

3 means for turning each subpixel ON by applying at least one voltage ramp to at
4 least one pair of sustain electrodes to create a standardized charge at each
5 subpixel; and

6 means for selectively removing said charge from at least one subpixel by applying
7 an erase pulse to its corresponding wire address electrode, thereby turning
8 said at least one subpixel OFF.

1 18. An electronic display comprising at least one fiber including at least one wire electrode
2 wherein said wire electrode is brought out through a seal region for direct
3 connection to a drive control system;

4 wherein said drive control system is selected from the group consisting of:

5 a) an erase drive control system;

6 b) a write address drive control system; and

7 c) a ramped voltage address drive control system..

1 19. The surface discharge plasma display device of claim 18, wherein said erase drive
2 control system includes:

3 means for storing a charge over said sustain electrodes on each subpixel to turn
4 each subpixel ON; and

5 means for selectively removing said charge from at least one subpixel by applying
6 an erase pulse to its corresponding wire address electrode, thereby turning
7 said at least one subpixel OFF.

1 20. The surface discharge plasma display device of claim 18, wherein said write address
2 drive control system includes:

3 means for removing a charge from each subpixel, thereby turning each subpixel
4 OFF; and

5 means for adding charge to at least one subpixel by applying a voltage to its
6 corresponding wire sustain electrodes and wire address electrode, thereby
7 turning said at least one subpixel ON.

1 21. The surface discharge plasma display device of claim 18, wherein said ramped voltage
2 drive control system includes:

- 3 means for turning each subpixel ON by applying at least one voltage ramp to at
4 least one pair of sustain electrodes to create a standardized charge at each
5 subpixel; and
- 6 means for selectively removing said charge from at least one subpixel by applying
7 an erase pulse to its corresponding wire address electrode, thereby turning
8 said at least one subpixel OFF..